IN THE CLAIMS:

Please substitute the following claims for the same numbered claims in the application.

Claim 1 (Currently Amended): A memory structure comprising:

a plurality of adjacent substrates stacked one on another;

a plurality of connectors connecting said substrates to one another;

a memory chip package mounted on each of said substrates; [[and]]

a first gap between a top of said memory chip package and a bottom of an adjacent substrate[[,]];

wherein said connectors have a size sufficient to form a [[space]] second gap between said substrates[[, and]];

wherein said [[space]] second gap is larger than a height of said memory chip package[[.]]; and

wherein said connectors comprises solder balls arranged in a fine ball grid array.

Claim 2 (Original): The memory structure in claim 1, wherein said memory chip package comprises a pre-tested memory chip package that is tested for defects before being mounted on said substrates.

Claim 3 (Original): The memory structure in claim 1, wherein said memory chip package and said substrates include identical electrical connections.

Claim 4 (Original): The memory structure in claim 1, wherein each of said substrates has a

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plurality of said memory chip packages mounted thereon.

Claim 5 (Cancelled).

Claim 6 (Previously Claimeded): The memory structure in claim 1, further comprising a thermal material between a top of said memory chip package and a bottom of an adjacent substrate.

Claim 7 (Original): The memory structure in claim 1, wherein said memory chip package comprises a chip having an array of memory elements mounted within a package.

Claim 8 (Currently Amended): A memory structure comprising:

a plurality of adjacent substrates stacked one on another;

a plurality of connectors connecting said substrates to one another;

a memory chip package mounted on each of said substrates; [[and]]

a first gap between a top of said memory chip package and a bottom of an adjacent substrate[[,]];

wherein said connectors have a size sufficient to form a [[space]] second gap between said substrates[[,]];

wherein said [[space]] second gap is larger than a height of said memory chip package, [[and]];

wherein each memory chip package includes only a single memory chip[[.]]; and

wherein said connectors comprises solder balls arranged in a fine ball grid array.

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Claim 9 (Original): The memory structure in claim 8, wherein said memory chip package comprises a pre-tested memory chip package that is tested for defects before being mounted on said substrates.

Claim 10 (Original): The memory structure in claim 8, wherein said memory chip package and said substrates include identical electrical connections.

Claim 11 (Original): The memory structure in claim 8, wherein each of said substrates has a plurality of said memory chip packages mounted thereon.

Claim 12 (Cancelled).

Claim 13 (Previously Presented): The memory structure in claim 8, further comprising a thermal material between a top of said memory chip package and a bottom of an adjacent substrate.

Claim 14 (Original): The memory structure in claim 8, wherein said memory chip package comprises a chip having an array of memory elements mounted within a package.

Claims 15-20 (Cancelled).

Claim 21 (Currently Amended): A vertically stacked memory module comprising:

a plurality of adjacent substrates stacked one on another;

a plurality of substrate spacers electrically connecting said substrates with one another;

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a single memory chip package mounted on each of said substrates;

a plurality of package spacers connecting said memory chip package with said substrates; [[and]]

a first gap between a top of said memory chip package and a bottom of an adjacent substrate[[,]];

wherein said memory chip package comprises a memory chip having an array of memory elements mounted within said package[[,]];

wherein said substrate spacers form a [[space]] second gap between a top of said memory chip package and a bottom of said adjacent substrates[[, and]];

wherein said [[space]] second gap is greater than a height of said memory chip package[[.]]; and

wherein said substrate spacers and said package spacers comprise solder balls arranged in a fine ball grid array.

Claim 22 (Previously Presented): The memory module in claim 21, wherein said memory chip package comprises a pre-tested memory chip package that is tested for defects before being mounted on said substrates.

Claim 23 (Previously Presented): The memory module in claim 21, wherein said memory chip package and said substrates include identical electrical connections.

Claim 24 (Previously Presented): The memory module in claim 21, wherein each of said substrates has a plurality of said memory chip packages mounted thereon.

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Claim 25 (Cancelled).

Claim 26 (Previously Presented): The memory module in claim 21, further comprising thermal material between a top of said memory chip package and a bottom of an adjacent substrate.

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